

## LH79520 System-On-Chip LCD Interfacing Guide

*Jun Li, Applications Engineer*

### PURPOSE

SHARP's LH79520 System-On-Chip design has an integrated LCD controller. It is able to directly interface to several different types of LCDs — STN, TFT and HR-TFT — without need for a separate LCD controller chip. This Application Note will show how to interface several different types of Liquid Crystal Displays with SHARP's LH79520 SoC, and provide detailed information about the LH79520 LCD controller to supplement the LH79520 User's Guide. Other information is included as a brief tutorial for the user who is unfamiliar with LCDs and LCD controllers.

### INTRODUCTION

#### LCD Technology

There are two common LCD technologies in use today. The first is Twisted Nematic (TN) technology which, building on the original Nematic technology, offers improved contrast. Developments in this type of technology include Super Twisted Nematic (STN) LCDs and Double Super-twisted Nematic Display (DSTN) LCDs.

The second type of technology in use today is Thin Film Transistor (TFT) technology. In this case, the front surface of the display is coated with a continuous electrode while the rear surface electrode is patterned into individual pixels. A thin film transistor (TFT) acts as a switch for each pixel. Improvements to this technology include SHARP's own HR-TFT (Highly Reflective Thin Film Transistor) LCDs.

Of the two technologies, TN technology is regarded as older technology and TFT is newer technology. TFT panels feature a wider viewing angle and fast response time (resulting in smoother moving picture displays). In particular, the HR-TFT LCD is a good choice for high ambient light conditions, such as outdoor usage because the more ambient light available for an HR-TFT LCD, the brighter HR-TFT LCD images appear.

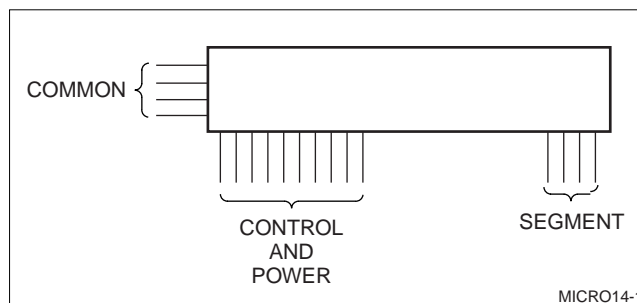
### LCD Interfacing

#### CHARACTER LCDs

There are a number of ways of interfacing simple Character LCD panels into low-end applications like calculators and toys. These applications use simple glass sandwich LCDs, so they require a minimum from their controller chips. The only complicated waveform required from the CPU or LCD control chip is an AC squarewave for bias on the LCD. The wire interface for those panels is frequently like the one in Figure 1.

This type of interface is called a Segment-Common interface. The control logic sends out 'Segment' signals along with one line of 'Common' signals. The refresh rate on these Common signals is about 50 Hz to 100 Hz.

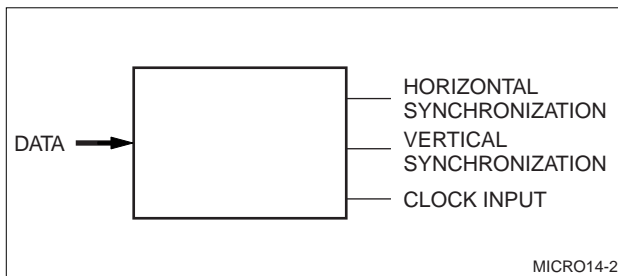
This interface method is common for character-type glass sandwich LCDs. Most character LCDs of this type are part of a panel assembly which includes the controller. To generate a display, the system just writes to the character LCD panel as a general 8-bit I/O port because the LCD controller in the panel handles the display and refresh tasks.



**Figure 1. Typical Character LCD Panel Interfacing**

## IMAGE LCDS

An Image LCD can display images instead of displaying characters only, as in the case of the Character LCD. The Image LCD is a higher resolution panel (LCD assembly inside a metal enclosure). These panels usually contain some flip-flop gates to reduce the number of data lines required, but require an external controller to refresh the data. The color depth for these panels can be anywhere from 1-bit (black and white — two colors), through 2-bit (gray, four colors), 4-bit (16 colors), 8-bit, 16-bit, and 24-bit color; the color depth corresponding to the number of input data lines for the LCD. A typical interface scheme is found in Figure 2.



**Figure 2. Typical Color Panel Interface Scheme**

### EXAMPLE WITH 160 × 120 MONOCHROME PANEL

For this 160 × 120 Monochrome panel example, there is only one data line, (D0) on the panel. To create a display, the LCD controller sets 160 clock pulses to the panel to latch 160 values for D0 for one (horizontal) line. After that, the LCD Controller sets the Horizontal Synchronization pulse HIGH to inform the LCD that one line of data is finished. The LCD panel latches this line of data and displays it on the screen. The controller moves on to the second line of data, continuing until all 120 vertical lines of data have been output to the LCD. Then the LCD Controller sets the Vertical Synchronization pulse HIGH to inform the LCD that one frame of data is transferred. The LCD panel resets its row (vertical) counter and the next line of input data will once again be the first line on the LCD. The vertical data refresh frequency and the Vertical Synchronization signal are about 50 Hz to 100 Hz in order to eliminate visible artifacts in the form of flicker.

The number of input data lines on any given panel usually corresponds to the color bit depth specified for the panel — a 1-bit LCD will have one data line, a 2-bit LCD will have two data lines, a 16-bit LCD will have 16 data lines, and so on.

Most Image-type LCD panels require a separate LCD controller to move the data from memory to the LCD panel as described above. This is normally achieved by a separate LCD controller chip or by using a SoC like SHARP's LH79520.

## TFT LCD SIGNALS

LCD panels unfortunately follow no uniform signal naming convention nor pin arrangement, so different LCD panels from different manufacturers will frequently have different pin arrangements and naming conventions. Pairing a Controller with an LCD will become much easier, once the required types of signals can be known and understood.

To help gain this understanding, this Application Note will use three different SHARP LCD panels for examples. It will also show how STN, TFT, and HR-TFT panels differ in signal and connection requirements, and to provide a basis for deciphering typical signals and connections used in LCD panels.

Table 1 shows a TFT LCD signal and pin description from a typical LCD manual. The example used here is the SHARP LQ057Q3DC02. All of these manuals are available on SHARP's website: [www.sharpsma.com](http://www.sharpsma.com).

These signals follow three categories: control signals, data signals, and power connections.

### Control Signals

The example in Table 1 shows control signals common to all LCD panels; again, they may differ by type and manufacturer:

- Clock signals (CK) for shifting RGB data into the LCD panel.
- Horizontal Synchronization signals (Hsync). There are 'N' number of CK periods per Hsync period where 'N' is the number of RGB pixels in a line. This signal marks the point at which the current line ends, and the new line begins.
- Vertical Synchronization signals (Vsync). There are 'M' number of Hsync periods per Vsync period where 'M' is the number of vertical lines in the display. This signal marks the point at which the current frame ends, and the new frame begins.

CK is the LCD's clock source, a continuous square-wave. The frequency must be correct and within the panel's specification to avoid flickering.

The Horizontal Synchronization signal is a pulse that is activated when one line of data has been transmitted to the LCD.

The Vertical Synchronization signal is a pulse that is activated when one page (or frame) of data has been transmitted to the LCD.

The clock frequency must be correct and the Synchronization signal polarities must be correct, otherwise the image on the LCD will exhibit twisting or flickering.

Table 1. Typical LCD TFT Panel Signals

PIN NO.	SYMBOL	I/O	FUNCTION
1	GND		Ground
2	CK	I	Data Sampling Clock
3	HSync	I	Horizontal Synchronizing signal (negative-going)
4	VSync	I	Vertical Synchronizing signal (negative-going)
5	GND		Ground
6	R0	I	Red Data Signal (LSB)
7	R1	I	Red Data Signal
8	R2	I	Red Data Signal
9	R3	I	Red Data Signal
10	R4	I	Red Data Signal
11	R5	I	Red Data Signal (MSB)
12	GND		Ground
13	G0	I	Green Data Signal (LSB)
14	G1	I	Green Data Signal
15	G2	I	Green Data Signal
16	G3	I	Green Data Signal
17	G4	I	Green Data Signal
18	G5	I	Green Data Signal (MSB)
19	GND		Ground
20	B0	I	Blue Data Signal (LSB)
21	B1	I	Blue Data Signal
22	B2	I	Blue Data Signal
23	B3	I	Blue Data Signal
24	B4	I	Blue Data Signal
25	B5	I	Blue Data Signal (MSB)
26	GND		Ground
27	ENAB	I	Horizontal Display Position Set Signal
28 - 29	VCC		+3.3 V
30	R/L	I	Horizontal Display Direction Select Signal L = Normal H = Reverse
31	U/D	I	Vertical Display Direction Select Signal L = Normal H = Reverse
32	V/Q	I	VGA/QVGA Mode Select Signal
33	GND		Ground

Other control signals for this TFT LCD are:

- ENAB: Enable signal
- R/L: Right or Left scan direction select
- U/D: Up or Down scan direction select
- V/Q: VGA or QVGA select

The Enable signal enables the LCD; and so must be HIGH to enable the LCD display.

Some control signals are specific to certain LCDs. In the sample above, R/L, U/D, V/Q signals must be tied to VCC or GND. They affect the image presentation (such as mirror imaging) and may not be available on all LCD panels.

### Data Signals

The data signals are:

- Blue[5:0]
- Green[5:0]
- Red[5:0]

There are 18 data signals in total. They correspond to the LCD controller or LH79520 SoC output LCDVD[17] to LCDVD[0]. These signals are the LCD image data; they are active between the Horizontal Synchronization (Hsync) and Vertical Synchronization (VSync) pulses.

### Power Connections

The LCD panel in this example requires VCC (3.3 V or 5 V) and GND.

## STN LCD SIGNALS

Table 2 shows an STN LCD signal and pin description from a SHARP LM057QCTT03 color STN LCD display.

**Table 2. Typical STN LCD Panel Signals**

PIN NO.	SYMBOL	DESCRIPTION	SIGNAL DIRECTION
1	YD	Scan Start	'1' to start scan
2	LP	Input Latch	Negative-going
3	XCK	Data Input Clock	Negative-going
4	DISP	Display Enable	'1' enables display
5	VDD	Logic Power	
6	VSS	Ground	
7	VEE	LCD Power	
8	D7	Display Data	1 = Dot ON 0 = Dot OFF
9	D6		
10	D5		
11	D4		
12	D3		
13	D2		
14	D1		
15	D0		

## Control Signals

The four control signals for this LCD are recognizable, when comparing them to the control signals in the TFT LCD panel:

- XCK = CK or CLOCK signal
- LP = Hsync or Horizontal Synchronization signal
- YD = Vsync or Vertical Synchronization signal
- DISP = ENAB or Enable signal

XCK is the LCD clock source, the same type of square wave for clocking data into the LCD panel.

The Horizontal Synchronization signal is a pulse activated when one line of data has been transmitted to the LCD.

The Vertical Synchronization signal is a pulse activated when one frame (or page) of data has been transmitted to the LCD.

The Enable signal enables the LCD; it must be HIGH to enable the LCD display.

Just as with the TFT LCD panel in the previous example, the clock frequency must be correct and the polarities of the Horizontal and Vertical Synchronization signal must be correct, otherwise the image on the LCD will exhibit twisting or flicker.

## Data Signals

The data signals are D[7:0], for a total of eight data lines corresponding to LCD controller output LCDVD[7] to LCDVD[0]. Just as with the TFT panel in the previous example, these signals are the LCD image data; they are active between the Horizontal Synchronization (Hsync) and Vertical Synchronization (VSync) pulses.

## Power Connections

The LCD panel in this example requires VCC (3.3 V or 5 V), GND and a VEE supply, typically 21 V - 24 V.

## HR-TFT SIGNALS

Table 3 shows an HR-TFT LCD signal and pin description from a SHARP LQ039Q2DS02 HR-TFT LCD.

**Table 3. Typical HR-TFT LCD Signals**

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	VDD		Gate Driver Power Supply
2	VCC		Gate Driver Logic Supply
3	MOD	I	Gate Driver Control Signal
4	MOD	I	Gate Driver Control Signal
5	U/L	I	Vertical Scan Direction Select
6	SPS	I	Gate Driver Control Signal

**Table 3. Typical HR-TFT LCD Signals (Cont'd)**

PIN NO.	SYMBOL	I/O	DESCRIPTION
7	CLS	I	Gate Driver Clock Signal
8	VSS		Gate Driver Logic Supply
9	VEE		Gate Driver Power Supply
10	VEE		Gate Driver Power Supply
11	VCOM	I	Common Electrode Drive Signal
12	VCOM	I	Common Electrode Drive Signal
13	SPL	I/O	Sampling Start Signal
14	R0	I	Red Data Signal (LSB)
15	R1	I	Red Data Signal
16	R2	I	Red Data Signal
17	R3	I	Red Data Signal
18	R4	I	Red Data Signal
19	R5	I	Red Data Signal (MSB)
20	G0	I	Green Data Signal (LSB)
21	G1	I	Green Data Signal
22	G2	I	Green Data Signal
23	G3	I	Green Data Signal
24	G4	I	Green Data Signal
25	G5	I	Green Data Signal (MSB)
26	B0	I	Blue Data Signal (LSB)
27	B1	I	Blue Data Signal
28	B2	I	Blue Data Signal
29	B3	I	Blue Data Signal
30	B4	I	Blue Data Signal
31	B5	I	Blue Data Signal (MSB)
32	VSHD		Digital Power Supply
33	DGND		Digital Power Supply
34	PS	I	Power Save Signal
35	LP	I	Data Latch Pulse from source
36	DCLK	I	Data Sampling Clock
37	LBR	I	Horizontal Scan Direction Signal
38	SPR	I/O	Sampling Start Signal
39	VSHA		Analog Power Supply
40	V0	I	Grayscale Voltage Standard
41	V1	I	Grayscale Voltage Standard
42	V2	I	Grayscale Voltage Standard
43	V3	I	Grayscale Voltage Standard
44	V4	I	Grayscale Voltage Standard
45	V5	I	Grayscale Voltage Standard
46	V6	I	Grayscale Voltage Standard
47	V7	I	Grayscale Voltage Standard
48	V8	I	Grayscale Voltage Standard
49	V9	I	Grayscale Voltage Standard
50	AGND		Analog Ground

### NOTES:

1. When U/L is '1', Normal scanning (top to bottom) occurs. When U/L is '0', Inverted scanning (bottom to top) occurs.
2. Horizontal Scanning inversion requires the interaction of three signals. See Table 4.

**Table 4. HR-TFT Horizontal Scanning Direction Select**

LBR	SPL	SPR	SCAN DIRECTION
1	Input	Output	Normal (left to right)
0	Output	Input	Reversed (right to left)

## Control Signals

HR-TFT panels (refer to Table 3) add several new control signals specific to their electronics, but still contain familiar signals:

- DCLK is similar to CK or CLOCK signals
- LP is similar to Hsync or Horizontal Synchronization signals
- SPS is similar to Vsync or Vertical Synchronization signals

DCLK (Dot Clock) is the clock source for the LCD. In HR-TFT panels, it is a square wave active only when data is valid. It is not a continuous waveform as in STN or TFT panels. But like STN and TFT panels, the clock frequency must be correct and conform to the panel specifications to avoid flickering.

The LP (Line Pulse) is similar to the Horizontal Synchronization signal, which is a pulse activated when one line of data has been transmitted to the LCD.

The SPS (Start Panel Sync) signal is similar to a Vertical Synchronization signal which is a pulse activated when one page (or frame) of data has been transmitted to the LCD.

Just as with the STN and TFT panels in the previous examples, the clock frequency must be correct and the polarities of the Horizontal and Vertical Synchronization signal must be correct, otherwise the image on the LCD will exhibit twisting or flicker.

Signals specific to HR-TFT panels begin with the CLS (Clock and Sync) signal. This is the clock signal for the row gate drivers. The repetition rate is similar to the Horizontal Synchronization signal, but it carries different setup and hold requirements.

The PS signal is the source driver control signal. The repetition rate and waveshape is the same as CLS, but with the polarity reversed.

The SPL (Start Pulse Left) pulse is the source driver's start signal. Its repetition rate is tied to the Horizontal Synchronization signal, and it occurs just after the Horizontal Synchronization pulse, to indicate the first valid data for the line.

SPR (Start Pulse Right) has the same function and repetition rate as SPL. These two signals are mutually exclusive, in that they are used in conjunction with LBR to decide the horizontal scan direction. When SPL is used for starting the signal output for source driver, the scan begins on the left side of the panel. When SPR is used, the scan begins on the right side of the panel. See Table 4.

LBR (Left Begin) is used in conjunction with SPR and SPL to decide the horizontal scan direction. When HIGH, the scan begins on the left, and SPL indicates the beginning of valid data for the line.

MOD is a control signal which must be HIGH to turn on the LCD.

U/L is the vertical scan direction select signal. When HIGH, the scan begins at the upper section of the panel.

CLS, PS, and SPL (or SPR) are signals generated by the HR-TFT controller. They are necessary for the HR-TFT LCD to operate. The LH79520, with its built-in LCD controller, can generate the necessary signals to operate any of the LCD panels in these examples.

## Data Signals

The data signals are:

- Blue[5:0]
- Green[5:0]
- Red[5:0]

There are 18 data signals corresponding to the LCD controller output LCDVD[17:0]. Image data is output on these lines, and being data, they are active between the Horizontal Synchronization pulses.

When connecting the SHARP LH79520 SoC to an HR-TFT display, the LH79520 only has 15 data lines available because the other three data lines are multiplexed to HR-TFT control signals when the System-On-Chip is in HR-TFT mode.

To make the interface to the LQ039Q2DS02 LCD work correctly, connect the 15 data lines from the LH79520 to the B[5:1], G[5:1], and R[5:1] lines, then tie B[0], G[0], and R[0] together with the intensity data line of the LH79520. This method will work well with any combination of panel and controller, where there are more data lines than controller chip outputs.

The disadvantage to this scheme is that only  $2^5 \times 2^5 \times 2^5 \times 2 = 65536$  colors are available from the LH79520 in HR-TFT mode instead of using the LCD's full capability of  $2^6 \times 2^6 \times 2^6 = 262,144$  colors.

## Power Connections

There are several power connections required for HR-TFT panels:

- VDD: High voltage, about +13.6 V
- VCC: High voltage, about -11.7 V
- VSS: High voltage, about -15 V
- VEE: Modulated squarewave voltage with a DC component of -9 V and an AC component of about 5 V
- VCOM: Derivative voltage from VEE with a DC component of about 1.4 V and an AC component of about 5 V. It is usually adjustable to allow for contrast differences in LCDs.
- VSHD: Digital logic voltage at either 3.3 V or 5 V
- VGND: Digital Ground
- VSHA: Analog logic voltage at either 3.3 V or 5 V
- AGND: Analog Ground
- V[9:0]: Grayscale voltage generated from a grayscale chip.

Detailed power supply requirements for the SHARP LQ039Q2DS02 panel can be found in the Device Specifications, available through your local SHARP dealer.

## LH79520 SoC (LCD CONTROLLER) OUTPUT SIGNALS

There are a total of 29 pins on the LH79520 System-On-Chip for LCD control and data functions. Table 5 details the LCD control functions in the SoC.

The signals listed in Table 5 are multiplexed with General Purpose I/O (GPIO) pins, and default to that function after reset. To use the LCD Controller functions of the LH79520, change the values in the LCDMux register.

The LCDMux register (address 0xFFFE5004) configures the set of LH79520 pins as either GPIO (the default upon reset) or as LCD interface pins. This is shown in further detail in Table 6.

Note that several of the bit fields in the LCDMux register configure more than one function (e.g. Bits 5:4 can configure pin 139 as 3 different functions). By changing the configuration of those bits, the LH79520 will output different signals to interface with STN, TFT and HR-TFT panels. This register is configured (see the Function column) based on what LCD will be connected to the LH79520.

**Table 5. LH79520 LCD Interface**

SIGNAL NAME	TYPE	DESCRIPTION
LCDVD[17:0]	Output	LCD Panel Data bus
LCDENAB	Output	LCD Data Enable
LCDFP	Output	Frame Pulse (STN), Vertical Synchronization Pulse (TFT)
LCDLDP	Output	Line Synchronization Pulse (STN), Horizontal Synchronization Pulse (TFT)
LCDDSPLEN	Output	LCD Panel Display Enable
LCDDCLK	Output	LCD Panel Data Clock
LCDCLKIN	Input	LCD External Clock Input
LCDVDDEN	Output	LCD Digital Supply Enable
LCDCLS	Output	LCD Clock Signal for Gate Driver (HR-TFT only)
LCDSPLS	Output	LCD Reset Signal for Row Display (HR-TFT only)
LCDREV	Output	LCD Reverse Signal (HR-TFT only)
LCDSPL	Output	LCD Line Start Pulse (Left) (HR-TFT only)
LCDPS	Output	LCD Power Save (HR-TFT only)

Table 6. LCDMux Register Bit Fields

BITS	FIELD NAME	FUNCTION
31:29	///	Reserved — Write '0'. Read '0'.
28	PIN114	1 = LCDVD11 0 = INT7 (reset)
27	PIN115	1 = LCDVD10 0 = INT6 (reset)
26	PIN116	1 = LCDVD9 0 = PD7 (reset)
25	PIN117	1 = LCDVD8 0 = PD6 (reset)
24	PIN118	1 = LCDVD7 0 = PD5 (reset)
23:22	PIN119	0b11 = Reserved — Write '0'. Read '0'. 0b10 = Configure the pin to function as LCDPS (HR-TFT panels) 0b01 = Configure the pin as LCDVD6 (STN panels) 0b00 = Configure the pin to function as PD4 (reset)
21	PIN121	1 = LCDVD5 0 = PD3 (reset)
20	PIN122	1 = LCDVD4 0 = PD2 (reset)
19	PIN123	1 = LCDVD3 0 = PD1(reset)
18	PIN124	1 = LCDVD2 0 = PD0 (reset)
17:16	PIN129	0b11 = Reserved — Write '0'. Read '0'. 0b10 = Configure the pin to function as LCDSPS (HR-TFT panels) 0b01 = Configure the pin to function as LCDFP (STN and TFT panels) 0b00 = Configure the pin to function as PC7 (reset)
15	PIN130	1 = LCDVD17 0 = PC6 (reset)
14:13	PIN131	0b11 = Reserved — Write '0'. Read '0'. 0b10 = Configure the pin to function as LCDLP (TFT and HR-TFT panels) 0b01 = Configure the pin to function as LCDLLP (STN panels) 0b00 = Configure the pin to function as PC5 (reset)
12	PIN132	1 = LCDVD16 0 = PC4 (reset)
11	PIN133	1 = LCDDCLK 0 = PC3 (reset)
10	PIN134	1 = LCDCLKIN 0 = PC2 (reset)
9:8	PIN135	0b11 = Reserved — Write '0'. Read '0'. 0b10 = Configure the pin to function as LCDCLS (HR-TFT panels) 0b01 = Configure the pin to function as LCDVDDEN (STN and TFT panels) 0b00 = Configure the pin to function as PC1 (reset)
7:6	PIN137	0b11 = Reserved — Write '0'. Read '0'. 0b10 = Configure the pin to function as LCDSPL (HR-TFT panels) 0b01 = Configure the pin to function as LCDENAB (STN and TFT panels) 0b00 = Configure the pin to function as PC0 (reset)
5:4	PIN139	0b11 = Reserved — Write '0'. Read '0'. 0b10 = Reserved — Write '0'. Read '0'. 0b01 = Configure the pin to function as LCDVD15 0b00 = Configure the pin to function as PB7 (reset)
3	PIN140	1 = LCDVD14 0 = PB6 (reset)
2	PIN141	1 = LCDVD13 0 = PB5 (reset)
1:0	PIN142	0b11 = Reserved — Write '0'. Read '0'. 0b10 = Configure the pin to function as LCDREV (HR-TFT panels) 0b01 = Configure the pin to function as LCDVD12 (STN and TFT panels) 0b00 = Configure the pin to function as PB4 (reset)

**NOTE:** All bits are Read/Write.

## EXAMPLE CONFIGURATIONS USING THE LH79520

The following section will describe specifically how to set up the LH79520 for the three different types of LCD displays previously used as examples: TFT, STN, and HR-TFT.

### TFT Display Connection

The interconnections between SHARP's LQ057Q3DC02 TFT LCD and the LH79520 are shown in Table 7. This Table shows only the interconnection between the LH79520 SoC and the LCD panel, without addressing the other normal connections to the LCD, such as power supplies.

**Table 7. Interconnection between  
LH79520 and a TFT LCD**

LCD PIN NO.	LCD SYMBOL	LH79520 PIN NO.	LH79520 SYMBOL	LCDMux REGISTER SETTING
2	CK	133	LCDDCLK	CLCP
3	Hsync	131	LCDLP	CLLP
4	Vsync	129	LCDFP	CLFP
6	R0	127	LCDVD[0]	CLD[0]
7	R1	126	LCDVD[1]	CLD[1]
8	R2	124	LCDVD[2]	CLD[2]
9	R3	123	LCDVD[3]	CLD[3]
10	R4	122	LCDVD[4]	CLD[4]
11	R5	121	LCDVD[5]	CLD[5]
13	G0	119	LCDVD[0]	CLD[0]
14	G1	118	LCDVD[7]	CLD[7]
15	G2	117	LCDVD[8]	CLD[8]
16	G3	116	LCDVD[9]	CLD[9]
17	G4	115	LCDVD[10]	CLD[10]
18	G5	114	LCDVD[11]	CLD[11]
20	B0	142	LCDVD[0]	CLD[0]
21	B1	141	LCDVD[13]	CLD[13]
22	B2	140	LCDVD[14]	CLD[14]
23	B3	139	LCDVD[15]	CLD[15]
24	B4	132	LCDVD[16]	CLD[16]
25	B5	130	LCDVD[17]	CLD[17]
27	ENAB	137	LCDENAB	CLDEN

### STN Display Connection

The interconnections between SHARP's LM057QCTT03 Color STN LCD and the LH79520 are shown in Table 8. This Table shows only the interconnection between the LH79520 SoC and the LCD panel, without addressing the other normal connections to the LCD, such as power supplies.

**Table 8. Interconnection between  
LH79520 and a STN Display**

LCD PIN NO.	LCD SYMBOL	LH79520 PIN NO.	LH79520 SYMBOL	LCDMux REGISTER SETTING
3	XCK	133	LCDDCLK	CLCP
2	LP	131	LCDLP	CLLP
1	YD	129	LCDFP	CLFP
15	D0	127	LCDVD[0]	CLD[0]
14	D1	126	LCDVD[1]	CLD[1]
13	D2	124	LCDVD[2]	CLD[2]
12	D3	123	LCDVD[3]	CLD[3]
11	D4	122	LCDVD[4]	CLD[4]
10	D5	121	LCDVD[5]	CLD[5]
9	D6	119	LCDVD[6]	CLD[6]
8	D7	118	LCDVD[7]	CLD[7]
4	DISP	135	LCDVDDEN	CLVDDEN

## HR-TFT Display Connection

The interconnections between SHARP's LQ039Q2DS02 HR-TFT LCD and the LH79520 are shown in Table 9. This Table shows only the intercon-

nection between the LH79520 SoC and the LCD panel, without addressing the other normal connections to the LCD, such as power supplies.

**Table 9. Interconnection between LH79520 and an HR-TFT Display**

LCD PIN NO.	LCD SYMBOL	LH79520 PIN NO.	LH79520 SYMBOL	LCDMuxREGISTER SETTING
36	DCLK	133	LCDDCLK	CLCP
35	LP	131	LCDLP	CLP
6	SPS	129	LCDFP	CLSPS
14	R0	127	LCDVD[0]	CLD[0]
20	G0	127	LCDVD[0]	CLD[0]
26	B0	127	LCDVD[0]	CLD[0]
15	R1	126	LCDVD[1]	CLD[1]
16	R2	124	LCDVD[2]	CLD[2]
17	R3	123	LCDVD[3]	CLD[3]
18	R4	122	LCDVD[4]	CLD[4]
19	R5	121	LCDVD[5]	CLD[5]
34	PS	119	LCDVD[6]	CPS
21	G1	118	LCDVD[7]	CLD[7]
22	G2	117	LCDVD[8]	CLD[8]
23	G3	116	LCDVD[9]	CLD[9]
24	G4	115	LCDVD[10]	CLD[10]
25	G5	114	LCDVD[11]	CLD[11]
		142	LCDVD[12]	CLREV signal to grayscale chip
27	B1	141	LCDVD[13]	CLD[13]
28	B2	140	LCDVD[14]	CLD[14]
29	B3	139	LCDVD[15]	CLD[15]
30	B4	132	LCDVD[16]	CLD[16]
31	B5	130	LCDVD[17]	CLD[17]
7	CLS	135	LCDVDDEN	CLS
13	SPL	137	LCDENAB	CLSPL

**NOTE:** Grayscale chip not used in HR-TFT Panels.

## LCD Controller Configuration Registers

The LH79520 Color LCD Controller consists of two blocks, the LCD Controller, and the HR-TFT controller. The LCD Controller block provides all necessary control and data signals to interface the LH79520 directly to a variety of color and monochrome LCD panels, including STN and TFT panels. The HR-TFT block modifies the output of the CLCDC to support HR-TFT panels.

Each type of LCD panel carries its own different set of requirements for input signals. To accommodate these

differing requirements, the LCD controller is configurable to output the correct signals with the correct sets of timings required by each different type of LCD panel.

By configuring the registers in the LH79520, its LCD controller is adaptable to different sizes, resolutions and different types of LCD panels. The configuration registers for the standard LCD controller in the LH79520 are listed in Tables 10 through 13. These Tables list both the Timing and Control registers, as they appear in the LH79520 User's Guide.

**Table 10. LCDTiming1 Register Bits**

BIT	FIELD NAME	DESCRIPTION
31:24	VBP	<b>Vertical Back Porch</b> VBP is the number of inactive lines at the start of a frame, after the vertical synchronization period. Program to '0' on passive displays or reduced contrast will result. The 8-bit VBP field is used to specify the number of line clocks inserted at the beginning of each frame. The VBP count starts just after the vertical synchronization signal for the previous frame has been negated for active mode, or the extra line clocks have been inserted as specified by the VSW bit field in passive mode. After this has occurred, the count value in VBP sets the number of line clock periods inserted before the next frame. VBP generates from 0 - 255 extra line clock cycles.
23:16	VFP	<b>Vertical Front Porch</b> VFP is the number of inactive lines at the end of frame, before the vertical synchronization period. Program to '0' on passive displays or reduced contrast will result. The 8-bit VFP field is used to specify the number of line clocks to insert at the end of each frame. Once a complete frame of pixels is transmitted to the LCD display, the value in VFP is used to count the number of line clock periods to wait. After the count has elapsed the vertical synchronization (CLFP) signal is asserted in active mode, or extra line clocks are inserted as specified by the VSW bit-field in passive mode. VFP generates from 0 - 255 line clock cycles.
15:10	VSW	<b>Vertical Synchronization (Pulse) Width</b> VSW is the number of horizontal synchronization lines. Program to the number of lines required minus one. Should be small (for example, program to '0') for passive STN LCDs. The higher the value, the worse the contrast on STN LCDs. The 6-bit VSW field is used to specify the pulse width of the vertical synchronization pulse. The register is programmed with the number of line clocks in VSync minus 1.
9:0	LPP	<b>Lines Per Panel</b> LPP is the number of active lines per screen. Program to the number of lines required minus 1. The LPP field specifies the total number of lines or rows on the LCD panel being controlled. LPP is a 10-bit value allowing between 1 and 1,024 lines. For dual panel displays, this register is programmed with the number of lines on each of the upper and lower panels.

Table 11. LCDTiming2 Register Bits

BIT	FIELD NAME	DESCRIPTION
31:27	///	Reserved — Should Be Zero
26	BCD	<b>Bypass Pixel Clock Divider</b> Setting this to '1' bypasses the pixel clock divider logic. This is mainly used for TFT displays.
25:16	CPL	<b>Clocks Per Line</b> This field specifies the number of actual CLCP clocks to the LCD panel on each line. This is the number of PPL divided by either 1 (TFT), 4 or 8 (for mono passive), 2-2/3 (for color passive), minus one. This must be correctly programmed in addition to PPL for the LCD controller to work correctly.
15	///	Reserved — Should Be Zero.
14	IOE	<b>Invert Output Enable</b> 0 = CLAC output pin is active HIGH in TFT mode 1 = CLAC output pin is active LOW in TFT mode  The Invert Output Enable (IOE) bit is used to select the active polarity of the output enable signal in TFT mode. In this mode, the CLAC pin is used as an enable that indicates to the LCD panel when valid display data is available. In active display mode, data is driven onto the LCD data lines at the programmed edge of CLCP when CLAC is in its active state.
13	IPC	<b>Invert Panel Clock</b> 0 = Data is driven on the LCD data lines on the rising-edge of CLCP 1 = Data is driven on the LCD data lines on the falling-edge of CLCP  The IPC bit is used to select the edge of the panel clock on which pixel data is driven out onto the LCD data lines.
12	IHS	<b>Invert Horizontal Synchronization</b> 0 = LP pin is active HIGH and inactive LOW 1 = LP pin is active LOW and inactive HIGH  The Invert HSync (IHS) bit is used to invert the polarity of the CLLP signal.
11	IVS	<b>Invert Vertical Synchronization</b> 0 = FP pin is active HIGH and inactive LOW 1 = FP pin is active LOW and inactive HIGH  The Invert VSync (IVS) bit is used to invert the polarity of the CLFP signal.
10:6	ACB	<b>AC Bias pin Frequency</b> The AC bias pin frequency is only applicable to STN displays, which require the pixel voltage polarity to be periodically reversed to prevent damage due to DC charge accumulation. Program this field with the required value minus 1 to apply the number of line clocks between each toggle of the AC bias pin (CLAC). This field has no effect if the CLCDC is operating in TFT mode, when the CLAC pin is used for the Data Enable signal.
5	CLKSEL	<b>Clock Select</b> This bit drives the CLCDCLKSEL signal, the select signal for the external LCD clock multiplexer.
4:0	PCD	<b>Panel Clock Divisor</b> The five-bit PCD field is used to derive the LCD panel clock frequency CLCP from the CLCDCLK frequency: $CLCP = CLCDCLK / (PCD + 2)$ . For mono STN displays with a four or eight-bit interface, the panel clock will be a factor of four and eight down on the actual individual pixel clock rate. For color STN displays, 2-2/3 pixels are output per CLCP cycle, hence the panel clock is 0.375 times. For TFT displays the pixel clock divider can be bypassed by setting the LCDTiming2[26] BCD bit.

Table 12. LCDTiming3 Register Bits

BIT	FIELD NAME	DESCRIPTION
31:17	///	Reserved — Should Be Zero
16	LEE	<b>LCD Line end enable</b> 0 = CLLE disabled (held LOW) 1 = CLLE signal active
15:7	///	Reserved — Should Be Zero
6:0	LED	<b>Line End Signal Delay</b> Line-End signal Delay from the rising edge of the last panel clock (CLCP). Program with number of CLCDCLK clock periods minus '1'.

Table 13. LCDControl Register Bits

BIT	FIELD NAME	DESCRIPTION
31:17	///	Reserved — Should Be Zero
16	WATERMARK	<b>LCD DMA FIFO Watermark Level</b> 0 = HBUSREQM is LOW when either of the two DMA FIFOs have four or more full locations. 1 = HBUSREQM is HIGH when either of the DMA FIFOs have eight or more empty locations.
15	LDmaFIFOTME	<b>LCD DMA FIFO Test Mode Enable</b> To be set only when LCD is disabled via bit 0 of this register. 0 = DMA FIFO inaccessible to user 1 = DMA FIFO read/write access for FIFO RAM testing.
14	///	Reserved — Should Be Zero
13:12	LcdVComp	<b>LCD Vertical Compare</b> Generates interrupt at: 00 = start of vertical synchronization 01 = start of back porch 10 = start of active video 11 = start of front porch
11	LcdPwr	<b>LCD Power Enable</b> 0 = LCD is off 1 = LCD is on when LCDEN = 1
10	BEPO	<b>Big-Endian Pixel Ordering</b> within a byte. The BEPO bit selects between little and big-endian pixel packing for 1, 2, and 4 bpp display modes, it has no effect on 8 or 16 bpp pixel formats. 0 = Little-endian ordering within a byte 1 = Big-endian pixel ordering within a byte
9	BEBO	<b>Big-Endian Byte Order</b> 0 = Little-endian byte order 1 = Big-endian byte order
8	BGR	<b>RGB or BGR Format Selection</b> 0 = RGB normal output 1 = BGR red and blue swapped
7	LcdDual	<b>LCD interface is Dual panel STN.</b> 0 = Single panel LCD is in use 1 = Dual panel LCD is in use
6	LcdMono8	<b>LCD is Monochrome with an 8-bit Interface</b> This bit controls whether monochrome STN LCD uses a 4 or 8-bit parallel interface. It has no meaning in other modes and for them should be programmed to '0'. 0 = Mono LCD uses 4-bit interface 1 = Mono LCD uses 8-bit interface
5	LcdTFT	<b>LCD is TFT</b> 0 = LCD is an STN display — use grayscale 1 = LCD is TFT — do not use grayscale
4	LcdBW	<b>STN LCD is monochrome (Black and White)</b> This bit has no meaning in TFT mode. 0 = STN LCD is color 1 = STN LCD is monochrome
3:1	LcdBpp	<b>LCD Bits Per Pixel</b> 000 = 1 bpp 001 = 2 bpp 010 = 4 bpp 011 = 8 bpp 100 = 16 bpp 101 = 24 bpp (TFT panel only) 110 = reserved 111 = reserved
0	LcdEn	<b>LCD controller Enable</b> LCD displays require that the LCD controller be running before power is applied to the LCD. For this reason, the LCD power-on control is not set to '1' unless both LCDEN and LCDPWR are set to '1'. Most LCD displays require the LCDEN to be set to 1 approximately 20 ms before LCDPWR is set to '1' for correct powering up. Likewise, LCDPWR should be set to '0' 20 ms before LCDEN is set to '0' for correct powering down. 0 = LCD controller disabled 1 = LCD controller enabled

## HR-TFT Controller

The configuration registers settings for the HR-TFT LCD controller are listed in Table 14 through Table 17.

**Table 14. LCDICPSetup Register Bits**

BITS	FIELD NAME	FUNCTION
31:16	///	Reserved — Should Be Zero
15:13	///	Reserved. Reads as '0'
12:4	PPL	Number of pixels per line. Program with (value required) - 1. Reset = '0'
3	VRVE	Reverse Vertical Scan. 1 = Normal Scanning 0 = Reverse Scanning Reset = '1'
2	HRVE	Horizontal Scan Reverse. 1 = Normal Scanning 0 = Reverse Scanning Reset = '1'
1:0	CR	Conversion mode select. 00 = Bypass Mode 01 = HR-TFT Mode 10 = Reserved 11 = Reserved Reset = '00'

**Table 15. LCDICPControl Register Bits**

BITS	FIELD NAME	FUNCTION
31:8	///	Reserved — Should Be Zero.
7	EN3	General purpose output enable 3
6	EN2	General purpose output enable 2
5	EN1	General purpose output enable 1
4	EN0	General purpose output enable 0
3	DISP	Controls the output of the display control signal DISP. Reset = 0
2	UBLEN	Controls the UBL tristate enable signal (UBLEN). Reset = 0
1	CLSEN	Controls the CLS tristate enable signal (CLSEN). Reset = 0
0	SPSEN	Controls the SPS tristate enable signal (SPSEN). Reset = 0

**Table 16. LCDICPTiming1 Register Bits**

BIT	FIELD NAME	DESCRIPTION
31:12	///	Reserved. Reads as '0'
11:8	PSDEL/CLSDEL	Controls the delay (number of LCDCLK periods) from the first detected LOW in the Hsync to the edge of the generated PS and CLS, program with (value required) -1. Reset = 0
7:4	REVDEL	Controls the delay (number of LCDCLK periods) from the first detected LOW in the Hsync to the falling edge of the generated REV signal, program with (value required) -1. Reset = 0
3:0	LPDEL	Controls the delay (number of LCDCLK periods) from the first detected LOW in the Hsync to the rising edge of the generated LP, program with (value required) -1. Reset = 0

**Table 17. LCDICPTiming2 Register Bits**

BIT	FIELD NAME	DESCRIPTION
31:16	///	Reserved - Should Be Zero
15:9	SPLVALUE	Sets the delay of the SPL and SPR pulses during vertical front and back porches. Note that this value must be programmed to a value greater than the HSW + HBP. Program with (value required -1). Reset = 0
8:0	PSDEL2/CLSDEL2	Controls the delay (the quantity of LCDCLK periods) from the first rising edge of SPL/SPR to the falling/rising edge of CLS/PS respectively. Program with (value required -1). Reset = 0

## ANALYSIS AND EXAMPLES

The control register descriptions in this Application Note are from the LH79520 System-On-Chip User's Guide. The following examples will provide insight into how these control registers operate. Values for these control registers will be derived by analysis of the LCD Data Sheets for timing and control signals.

When interfacing any LCD, consult the manufacturer's Data Sheet for the necessary timing and control information. Armed with this knowledge, a Designer can then interface the LH79520 with any type of LCD in the market from any manufacturer.

## Reading an LCD Waveform

When examining the LCD panel waveform specifications supplied by the LCD manufacturer, it will be noted that almost all of the LCD configuration registers can be determined from those waveforms.

### TFT DISPLAY EXAMPLE

The timing diagram for SHARP's LQ057Q3DC02 320 × 240 TFT LCD is shown in Figure 3. Its waveforms are similar to many other types of TFT LCDs.

Based on the timing diagrams provided by the LCD manufacturer, configuration register values can be determined, as shown in Table 18 through Table 22.

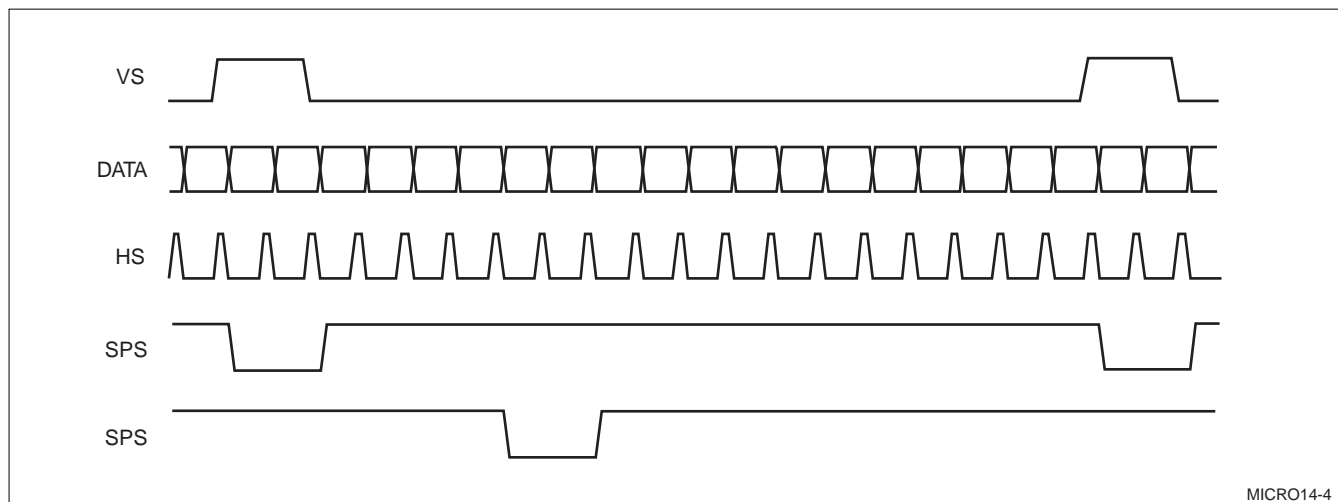


Figure 3. TFT Timing Diagram

Table 18. LCD Timing0 Register

BIT FIELD	VALUE	DESCRIPTION
HBP[31:24]	tHE	Horizontal back porch is 'tHE', the value between the edge of horizontal synchronization signal and the start of first data D1.
HFP[23:16]	tH-tHE-tHD	Horizontal front porch is 'tH-tHE-tHD', the value between the last data (D320) and the edge of the next horizontal synchronization signal.
HSW[15:10]	tHP	Horizontal synchronization pulse width is 'tHP'.
PPL[7:2]	19	Pixels-per-line is $320 = 16 \times (\text{PPL} + 1)$ , therefore the PPL value is '19'.

Table 19. LCDTiming1 Register

BIT FIELD	VALUE	DESCRIPTION
VBP[31:24]	tVH+tVS-tVP	Vertical back porch is 'tVH+tVS-tVP', the number of inactive lines at the start of a frame after vertical synchronization pulse.
VFP[23:16]	tV-tVH-tVS-tVD	Vertical front porch is 'tV-tVH-tVS-tVD', the number of inactive lines at the end of frame, before vertical synchronization pulse.
VSW[15:10]	tVP	Vertical synchronization pulse is 'tVP'.
LPP[9:0]	239	Lines per panel is the number of active lines per screen, and here the value is $240 - 1 = 239$ .

Table 20. LCD Timing2 Register

BIT FIELD	VALUE	DESCRIPTION
BCD[26]	0	Bypass pixel clock divider; the value is '0' to use the clock divider in the LCD controller.
CPL[25:16]	319	Clocks per line; here the value is $320 - 1 = 319$ .
IOE[14]	0	Invert output enable; here the value is '0' because the output enable signal is active HIGH.
IPC[13]	1	Invert panel clock; here the value is '1' because the data is driven on the falling edge of the clock.
IHS[12]	1	Invert horizontal synchronization; here the value is '1' because the horizontal synchronization signal is active LOW.
IVS[11]	1	Invert vertical synchronization; here the value is '1' because the vertical synchronization signal is active LOW.
ACB[10:6]	0	AC bias pin frequency; here the value is set to '0' because it does not apply to this panel.
CLKSEL[5]	0	Clock signal selection; here the value is '0' because we are using the SoC's internal clock.
PCD	6	Panel clock divisor; here the value is '6'. The required LCD clock is 6.3 MHz, so because the internal clock source for the LCD is 50 MHz, then $50 \text{ MHz} = 6.3 \text{ MHz} \times (\text{PCD} + 2)$ . This yields a value for PCD of '6'.

Table 21. LCDTiming3 Register

BIT FIELD	VALUE	DESCRIPTION
LEE[16]	0	LCD line end enable; here the value is '0' because it is not used.
LED[6:0]	0	Line-end signal delay from the rising-edge of the last panel clock; here the value is '0' because it is not used.

Table 22. LCDControl Register

BIT FIELD	VALUE	DESCRIPTION
WATERMARK[16]	0	LCD DMA FIFO Watermark level; here the value can be '0' unless a big DMA FIFO is required.
Ldma-FIFOTME[15]	0	LCD DMA FIFO test mode enable; this value must be '0' to set the DMA FIFO as inaccessible.
LcdV-Comp[13:12]	0	Generate interrupt; here the value is '0' to not use the interrupt for the LCD.
LcdPwr[11]	1	LCD power enable; here the value is '1' to turn on the LCD.
BEPO[10]	0	Big-endian pixel ordering within a byte; here the value is for little-endian ordering within a byte.
BEBO[9]	1	Invert vertical synchronization; here the value is '1' because the vertical synchronization signal is active LOW.
BGR[8]	0	RGB or BGR format selection; here the value is '1' because the code requires BGR output.
LcdDual[7]	0	LCD interface is dual panel STN; here the value is '0' because it does not apply.
LcdMono8[6]	0	Monochrome LCD has an 8-bit interface; here the value is '0' because it does not apply.
LCDTFT[5]	1	LCD is TFT; here the value is '1' because this is a TFT display.
LcdBW[4]	0	STN LCD is monochrome; here the value is '0' because it does not apply.
LcdBpp[3:1]	100b	LCD bits per pixel; here the value is 0x100 using the schematic design as in the LH79520 EVB is a 16-bit interface. The value can be '101' if the design is using a 24-bit interface.
LcdEn[0]	1	LCD controller enable; here the value is '1' to turn on the LCD.

**Display on LH79520 EVB**

After setting the LCDControl registers, the LQ057Q3DC02 TFT LCD on the LH79520 EVB will display the image, once the LCDUPBASE register (0xFFFF4010) is pointed to the image data in the memory.

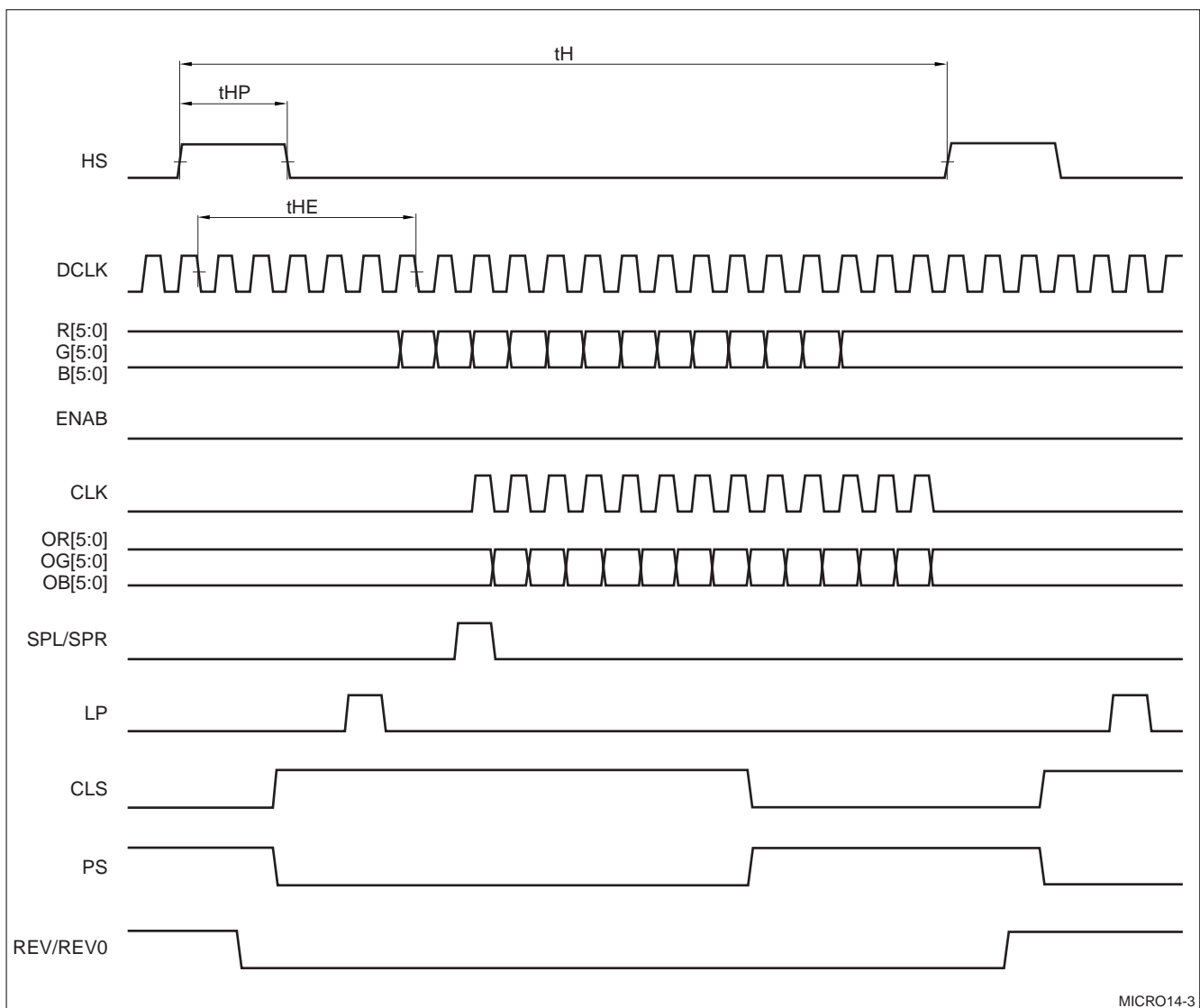
**HR-TFT DISPLAY**

The timing diagram for SHARP’s LQ039Q2DS02 320 x 240 HR-TFT LCD is shown in Figure 4; it is similar to many other types of HR-TFT LCDs.

The timing diagram for an HR-TFT display is composed of two parts. The first half defines the LCD controller parameters, which also contain the waveforms

for ENAB, HS and DCLK. The second half defines the parameters for the HR-TFT controller and also contains the waveforms for CLK through REV. Since the HR-TFT controller is connected internally to the LCD controller in the LH79520, and in this case the HR-TFT controller is active, the output waveform for the HR-TFT controller is output on the LH79520 external pins. The two controllers both have to be programmed correctly for this to occur.

Using the timing diagram provided by the LCD manufacturer, the LCD controller configuration register values can be determined by the first half of the waveform and are listed in Tables 23 and 24.



**Figure 4. HR-TFT Waveforms**

Table 23. LCDDTiming0 Register Values

BIT FIELD	VALUE	DESCRIPTION
HBP[31:24]	60	Horizontal Back Porch is approximately $72 \text{ DCLK} - 12 \text{ DCLK} = 60$ , the value between the edge of horizontal synchronization signal and the start of first data (D1).
HFP[23:16]	60	Horizontal Front Porch can initially be set to the same value as HBP if it is unclear from the waveform specifications and then it can be adjusted according to the amount of image shifting visible on the LCD screen. It is the value between the last data (D320) and the edge of the next horizontal synchronization signal.
HSW[15:10]	12	Horizontal Synchronization pulse Width is '12' as shown.
PPL[7:2]	19	Pixels-per-line is $320 = 16 \times (\text{PPL} + 1)$ , the PPL value is '19'.

Table 24. LCDDTiming1 Register Values

BIT FIELD	VALUE	DESCRIPTION
VBP[31:24]	3	Vertical Back Porch here is '3', the number of inactive lines at the start of a frame after the vertical synchronization pulse.
VFP[23:16]	4	Vertical Front Porch here is '4', the number of inactive lines at the end of frame, before the vertical synchronization pulse.
VSW[15:10]	0	Vertical Synchronization pulse Width here is '0'. Frequently a very small value; when experimenting, use values beginning at '0'.
LPP[9:0]	239	Lines Per Panel is the number of active lines per screen, here the value is $240 - 1 = 239$ .

**NOTE:** The values of VBP, VFP, and VSW are generally between 0 and 5. A bit of trial-and-error will get the best display result.

Table 25. LCDDTiming2 Register Values

BIT FIELD	VALUE	DESCRIPTION
BCD[26]	0	Bypass pixel Clock Divider, here the value is '0' to use (not bypass) the LCD clock divider.
CPL[25:16]	319	Clocks Per Line, here the value is $320 - 1 = 319$ .
IOE[14]	0	Invert Output Enable, here the value is '0' as the output enable signal is active HIGH.
IPC[13]	1	Invert Panel Clock, here the value is '1' as the data is driven on the falling edge of clock.
IHS[12]	0	Invert Horizontal Synchronization, here the value is '0' as the horizontal synchronization signal is active HIGH.
IVS[11]	0	Invert Vertical Synchronization, here the value is '0' as the vertical synchronization signal is active HIGH.
ACB[10:6]	0	AC Bias frequency, here the value is set to '0' because this panel does not require a bias.
CLKSEL[5]	0	Clock Signal Selection, here the value is '0' for using SoC internal clock.
PCD	8	Panel Clock Divisor, here the value is '6' in this case. The required LCD clock is 5 Mhz, therefore if the internal clock source for the LCD is 50 MHz; therefore $50 \text{ MHz} = 5 \text{ MHz} (\text{PCD} + 2)$ , PCD will then be '8'.

Table 26. LCDDTiming3 Register Values

BIT FIELD	VALUE	DESCRIPTION
LEE[16]	0	LCD Line End Enable, here the value is '0' because it is not used for this panel.
LED[6:0]	0	Line-end signal Delay from the rising-edge of the last panel clock, here the value is '0' because it is not used for this panel.

Table 27. LCDControl Register Values

BIT FIELD	VALUE	DESCRIPTION
WATERMARK[16]	0	LCD DMA FIFO Watermark level, here the value is '0' unless a large DMA FIFO is required.
Ldma-FIFOTME[15]	0	LCD DMA FIFO test mode enable, here the value must be '0' because this is a production test.
LcdV-Comp[13:12]	0	Generate interrupt; here the value is '0' to not use the LCD interrupt.
LcdPwr[11]	1	LCD power enable, a value of '1' turns on the LCD.
BEPO[10]	0	Big-endian pixel ordering within a byte, here the value is for little-endian ordering within a byte.
BEBO[9]	0	Invert vertical synchronization, here the value is '0' as vertical synchronization signal is active HIGH.
BGR[8]	1	RGB or BGR format selection, here the value is '1' as the panel requires BGR output.
LcdDual[7]	0	The connected LCD is dual panel STN, here the value is '0' for it does not apply to this panel.
LcdMono8[6]	0	The connected Monochrome LCD has an 8-bit interface, here the value is '0' because it does not apply.
LCDTFT[5]	1	The connected LCD is TFT, here the value is '1' because this is a TFT display.
LcdBW[4]	0	The connected STN LCD is monochrome, here the value is '0' because it does not apply.
LcdBpp[3:1]	100b	LCD bits per pixel, here the value is 100b because the design of the LH79520 EVB is a 16-bit interface. The value would be 101 if the design were a 24-bit interface.
LcdEn[0]	1	LCD controller enable; a value of '1' turns on the LCD.

## HR-TFT Controller Configuration Register Values

### SETUP REGISTER

- PPL: Number of pixels per line is  $320 - 1 = 0x13F$
- VRVE: Input to set up/down or reverse scanning. The value for normal scanning is '1'.
- HRVE: Input to set up right/left reverse scanning. The value for normal scanning is '1'.
- CR: Conversion mode select. The value is '01' for HR-TFT.

### CONTROL REGISTER

- EN3: General purpose output enable 3, value is '0'.
- EN2: General purpose output enable 2, value is '0'.
- EN1: General purpose output enable 1, value is '0'.
- EN0: General purpose output enable 0, value is '0'.
- DISP: controls the display control signal DISP, value is '1'.
- UBLLEN: Controls the UBL tristate enable, value is '0'.
- CLSEN: Controls the CLS tristate enable, value is '0'.
- SPSEN: Controls the SPS tristate enable, value is '0'.

### TIMING REGISTER 1

- PSDEL/CLSDEL: Controls the delay (number of LCDCLK periods) from the first detected LOW in Hsync to the edge of the generated PS and CLS, the value is 9 DCLK.
- REVDEL: Controls the delay (number of LCDCLK periods) from the first detected LOW in Hsync to the rising edge of the generated LP, the value is 3 DCLK.
- LPDEL: Controls the delay (number of the LCDCLK periods) from the first detected LOW in Hsync to the rising edge of the generated LP, the value is 14 DCLK.

### TIMING REGISTER 2

- SPLVALUE: Sets the delay of the SPL and SPR pulses during vertical front and back porches, the value is  $73 \text{ DCLK} - 1 = 72$ .
- PSDEL2/CLSDEL2: Controls the delay (the quantity of LCDCLK periods) from the first rising edge of SPL/SPR to the falling/rising edge of CLS/PS respectively, the value is 289 DCLK.

### STN Display

The timing diagram for SHARP's LM057QCTT03 320 x 240 Color STN LCD is shown in Figure 5; it is similar to many other types of Color STN LCDs.

Based on this timing diagram provided by the LCD manufacturer, the configuration register values can then be determined.

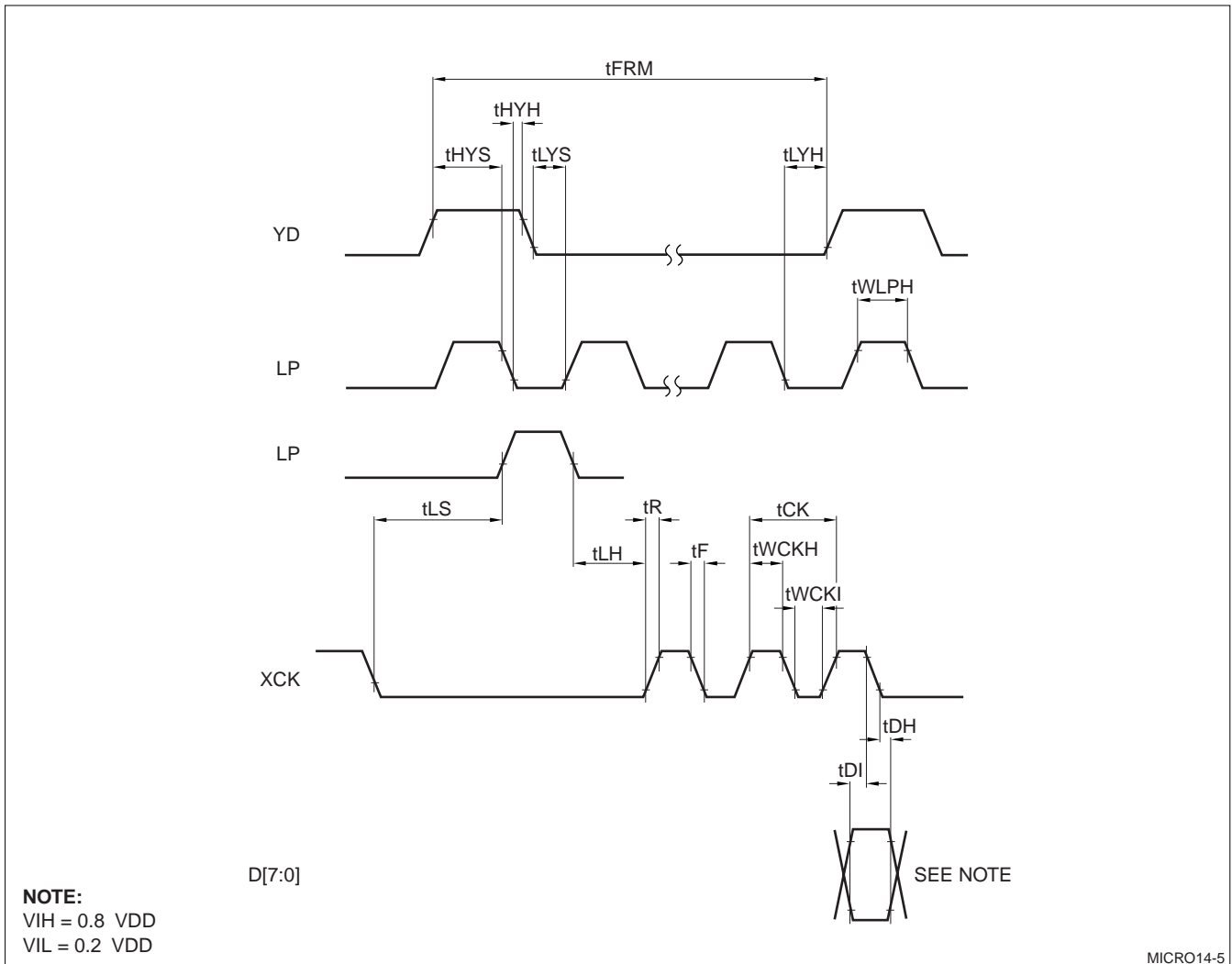


Figure 5. Color STN Display Waveforms

Table 28. LCDTiming0 Register Values

BIT FIELD	VALUE	DESCRIPTION
HBP[31:24]	tLH	Horizontal Back Porch is 'tLH', the value between the edge of horizontal synchronization signal and the start of first data (D1).
HFP[23:16]	tLS	Horizontal Front Porch is 'tLS', the value between the last data (D320) and the edge of next horizontal synchronization signal.
HSW[15:10]	tWLP	Horizontal Synchronization pulse Width is 'tWLPH'.
PPL[7:2]	19	Pixels-per-line is 320 = 16 x (PPL + 1), here the PPL value is '19'.

Table 29. LCDTiming1 Register Values

BIT FIELD	VALUE	DESCRIPTION
VBP[31:24]	1	Vertical Back Porch is '1', the number of inactive lines at the start of a frame after the vertical synchronization pulse.
VFP[23:16]	1	Vertical Front Porch is '1', the number of inactive lines at the end of frame, before the vertical synchronization pulse.
VSW[15:10]	0	Vertical synchronization Pulse Width is '0'; it must be '0' for an STN display.
LPP[9:0]	239	Lines Per Panel is the number of active lines per screen, here the value is $240 - 1 = 239$ .

**NOTE:** The value for VBP, VFP, and VSW is usually very small and VSW is normally '0' for STN displays.

Table 30. LCDTiming2 Register Values

BIT FIELD	VALUE	DESCRIPTION
BCD[26]	0	Bypass pixel Clock Divider, the value is '0' to use LCD clock divider.
CPL[25:16]	119	Clocks Per Line, the value is $(320 - 1) \times 3/8 = 119$ . Note that the formula differs from that required for a TFT panel.
IOE[14]	0	Invert Output Enable, the value is '0' as output enable signal is active HIGH.
IPC[13]	0	IPC: Invert Panel Clock, the value is '0' as data is driven on the rising edge of the clock.
IHS[12]	0	Invert Horizontal Synchronization, the value is '0' as the horizontal synchronization signal is active HIGH.
IVS[11]	0	Invert Vertical Synchronization, the value is '0' as the vertical synchronization signal is active HIGH.
ACB[10:6]	0	AC Bias frequency, the value is set to '0' because it does not apply.
CLKSEL[5]	0	Clock signal select, the value is '0' to use the SoC internal clock.
PCD	6	Panel Clock Divisor, the value is '6' in this case. The required LCD clock is 7.5 MHz, so if the internal clock source for the LCD is 50 MHz, so $50 \text{ MHz} = 7.5 \text{ MHz} \times (\text{PCD} + 2)$ , therefore the PCD will be '6'.

Table 31. LCDTiming3 Register Values

BIT FIELD	VALUE	DESCRIPTION
LEE[16]	0	LCD Line End Enable, the value is '0' because it is not used.
LED[6:0]	0	Line-end signal Delay from the rising-edge of the last panel clock, the value is '0' because it is not used.

Table 32. LCDControl Register Values

BIT FIELD	VALUE	DESCRIPTION
WATERMARK[16]	0	LCD DMA FIFO Watermark level, the value is '0' unless a large DMA FIFO is required.
Ldma-FIFOTME[15]	0	LCD DMA FIFO tLCD DMA FIFO test mode enable, here the value must be '0' because this is a production test.
LcdV-Comp[13:12]	0	Generate interrupt; the value is '0' to not use the LCD interrupt.
LcdPwr[11]	1	LCD power enable, the value is '1' to turn on the LCD.
BEPO[10]	0	Big-endian pixel ordering within a byte, here the value is for little-endian ordering within a byte.
BEBO[9]	0	Invert vertical synchronization, here the value is '0' as the vertical synchronization signal is active HIGH.
BGR[8]	1	RGB or BGR format selection, the value is '1' as the panel requires BGR output.
LcdDual[7]	1	The connected LCD is dual panel STN, the value is '1' since this STN panel is a single panel.
LcdMono8[6]	0	The connected Monochrome LCD has an 8-bit interface, the value is '0' because it does not apply.
LCDTFT[5]	0	The connected LCD is TFT, the value is '0' because this is an STN display.
LcdBW[4]	0	The connected STN LCD is monochrome, the value is '0' because it is color STN.
LcdBpp[3:1]	011b	LCD bits per pixel, the value is 011b to use the 256-color palette. The value is 010b to use the 16-color palette.
LcdEn[0]	1	LCD controller enable; here a value of '1' turns on the LCD.

## LH79520 LCD Controller Clocking

The LCD clock output signal on the LH79520 can be from two sources:

- From an external clock supply. The LCD Controller's External clock source can be selected by changing the CLKSEL bit in LCDTiming2 register and by changing the General Purpose I/O muxing to set pin 134 to LCDDCLKIN. The external clock source will pass through the divider (a BCD value in LCDTiming2 of '1' will bypass the divider) inside the LCD controller. The divider value is set by the value of PCD in the LCDTiming2 register.
- From an internal clock supply. In this case, the system clock HCLK (sometimes called Bus Clock) is the main source for the LCD controller. The HCLK passes through two dividers. The first divider is LCDClkPrescale in the RCPC controller block. It divides HCLK by 1, 2, 4, and so on, then feeds the clock to the LCD Controller. The second divider is the divider inside the LCD controller (a BCD value in LCDTiming2 of '1' will bypass the divider) inside the LCD controller. If used, the divider value is set by the PCD value in the LCDTiming2 register.

To use the internal clock, enable the clock bypass from the RCPC block to the LCD controller. The PeriphClkCtrl2 register bit 0 (in the RCPC controller block) controls this bypass. The value in this bit is '1' after reset, when changed to '0', it enables the clock to the LCD controller.

It then becomes important to know the value for HCLK. HCLK comes from the PLL via the HCLKPrescale divider. The recommended crystal for the LH79520 is 14.74 MHz; the PLL circuit in the SoC boosts this base frequency to about 310 MHz for a clock. The HCLK is derived from this 310 MHz clock; so if the HCLKPrescale value is '6', the HCLK will be  $310 \div 6 = 51.7$  MHz which is the maximum bus speed for this SoC.

## BANDWIDTH

The LCD controller system in the LH79520 can drive many types of LCDs — STN, TFT, HR-TFT and in different sizes. But there is an upper limit to the size, color depth, and refresh rate that it can drive. The large LCD panels require a lot of bandwidth from the LH79520. Bandwidth here means bus usage; the larger the panel, the more image information it requires.

For example, the maximum bus speed for the LH79520 is 50 MHz. The SoC can use 40 MHz of that 50 MHz to move data from memory to the LCD and the remaining 10 MHz for moving code and data from memory to the SoC for execution. As the LCD size gets larger, the SoC will be forced to use more bandwidth to move image data from memory to the LCD.

Consider the effects when driving an  $800 \times 600$  color LCD. The refresh rate for the panel is 70 Hz and the color depth used in this panel is 8 bits (1 byte). The SoC bus usage will be  $800 \times 600 \times 70 \times 1 = 33.6$  MHz for picture data alone, without considering the front porch and back porch delays required by the LCD. When the back porch and front porch delays are added, the bandwidth usage climbs.

Other bandwidth usage comes from memory fetch delays. There is no delay if the image is fetched from LH79520 internal memory. There will be some delay if the image is fetched from SDRAM and there will be a long delay if the image is fetched from SRAM. If slow SRAM is used to store this image, the bandwidth left for any other task drops rapidly toward 0.

The LH79520 has 32K internal memory, which can be used for storing images. But if the LCD size is  $800 \times 600$ , it will require ( $800 \times 600 = 468.75K$ ) memory; therefore any image will have to be stored in and fetched from external memory. If the LCD size is  $320 \times 240$  with 2 bits per pixel, then memory usage is ( $320 \times 240 \div 4 = 18.75K$ ) therefore that will fit in the internal memory. Detailed calculation tables for bandwidth usage are shown in Tables 33 and 34. These Tables are also good references for LCD panel size and pixel depth compatibility with the LH79520.

The bandwidth usage also climbs as the LCD refresh rate climbs.

**Table 33. LCD Data Requirements with 70 Hz Refresh, External LCD Clock, and ARM720T Bandwidth**

PANEL RESOLUTION WITH DATA REQUIREMENT		Frame Buffer (KB)	ATTAINABLE LCD DATA RATE			BUS BANDWIDTH NEEDED BY LCD			BANDWIDTH LEFT FOR OTHER OPERATIONS			EFFECTIVE CPU FREQUENCY		
						SDRAM	EXT SRAM	INT SRAM	SDRAM	EXT SRAM	INT SRAM	SDRAM	EXT SRAM	INT SRAM
Resolution H x V	Bits/Pixel		MPixels/s	MWords/s	MBursts/s	%	%	%	%	%	%	MHz	MHz	MHz
XGA: 1024 x 768 Requires 60.5526 Mpixels/s	1	96.00	60.5526	1.89	0.24	10.88	14.19	x	89.12	85.81	x	38.0	38.5	x
	2	192.00	60.5526	3.78	0.47	21.75	28.39	x	78.24	71.61	x	35.5	35.0	x
	4	384.00	60.5526	7.57	0.95	43.52	56.77	x	56.48	43.23	x	29.3	25.7	x
	8	768.00	60.5526	15.14	1.89	87.05	113.54	x	12.95	0.0	x	9.5	0.0	x
	16	1536.00	60.5526	30.28	3.78	174.10	227.08	x	0.0	0.0	x	0.0	0.0	x
SVGA: 800 x 600 Requires 36.96 Mpixels/s	1	58.59	36.96	1.16	0.14	6.64	8.66	x	93.36	91.34	x	38.9	39.8	x
	2	117.19	36.96	2.31	0.29	13.28	17.33	x	86.72	82.68	x	37.5	37.8	x
	4	234.38	36.96	4.62	0.58	26.57	34.65	x	73.44	65.35	x	34.3	33.3	x
	8	468.75	36.96	9.24	1.16	53.13	69.30	x	46.87	30.70	x	26.0	20.2	x
	16	937.50	36.960	18.48	2.31	106.26	138.60	x	0.0	0.0	x	0.0	0.0	x
VGA: 640 x 480 Requires 23.6544 Mpixels/s	1	37.50	23.6544	0.74	0.09	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	2	75.00	23.6544	1.48	0.18	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x
	4	150.00	23.6544	2.96	0.37	17.00	22.18	x	83.0	77.82	x	36.6	36.6	x
	8	300.00	23.6544	5.91	0.74	34.00	44.35	x	66.0	55.65	x	32.2	30.3	x
	16	600.00	23.6544	11.83	1.48	68.01	88.70	x	31.99	11.30	x	19.9	8.9	x
HVGA: 640 x 240 Requires 11.8272 Mpixels/s	1	18.75	11.8272	0.37	0.05	2.13	2.77	1.20	97.87	97.23	98.80	39.9	41.0	57.5
	2	37.50	11.8272	0.74	0.09	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	4	75.00	11.8272	1.48	0.18	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x
	8	150.00	11.8272	2.96	0.37	17.00	22.18	x	83.0	77.82	x	36.6	36.6	x
	16	300.00	11.8272	5.91	0.74	34.00	44.35	x	66.0	55.65	x	32.2	30.3	x
QVGA: 320 x 240 Requires 5.9136 Mpixels/s	1	9.38	5.9136	0.18	0.02	1.06	1.39	0.60	98.94	98.61	99.40	40.1	41.3	57.6
	2	18.75	5.9136	0.37	0.05	2.13	2.77	1.20	97.87	97.23	98.80	39.9	41.0	57.5
	4	37.50	5.9136	0.74	0.09	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	8	75.00	5.9136	1.48	0.18	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x
	16	150.00	5.9136	2.96	0.37	17.00	22.18	x	83.0	77.82	x	36.6	36.6	x
1/8 VGA: 320 x 120 Requires 2.9568 Mpixels/s	1	4.69	2.9568	0.09	0.01	0.53	0.69	0.30	99.47	99.31	99.70	40.2	41.4	57.6
	2	9.38	2.9568	0.18	0.02	1.06	1.39	0.60	98.94	98.61	99.40	40.1	41.3	57.6
	4	18.75	2.9568	0.37	0.05	1.71	2.23	0.97	97.87	97.23	98.80	39.9	41.0	57.5
	8	37.50	2.9568	0.74	0.09	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	16	75.00	2.9568	1.48	0.18	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x

**NOTES:**

- Internal SRAM: 32KB
- AHB Frequency: 50 MHz
- Burst size: 8 Words
- CLCD FIFO Fill Trigger → AHB Request: 1 Cycle
- AHB Request → Start AHB Access: 3 Cycles
- CLCD FIFO Data Load from AHB: 1 Cycle
- SDRAM burst: 23 Cycles (Controller input delay: 2 Cycles; Close old bank: 2 Cycles; Open new bank: 2 Cycles; CAS latency: 2 Cycles; Controller output delay: 2 Cycles)
- ARM SDRAM Controller is used
- Ext SRAM burst: 30 Cycles (Each word access: 3 Cycles; First word Overhead: 1 Cycle)
- ARM Static Memory Controller is used.
- Int SRAM burst: 13 Cycles
- CPU Speed 75 MHz
- Cache Hit/Miss Rate: 85%/15%
- ARM 720T Delay: 2 CPU Cycles

- AHB Wrapper Delay: 1 AHB Cycle
- Async Mode Delay: 2 1/2 CPU and 1/2 AHB Cycles
- All CPU accesses are cache line fills. (Burst size: 4; SDRAM burst: 14 Cycles; Ext. SRAM burst: 13 Cycles; Int. SRAM burst: 4 Cycles)
- MMU Hit Rate: 100.0%
- Effective CPU Frequency (MAX.): SDRAM: 40.3 MHz; External SRAM: 41.5 MHz; Internal SRAM: 57.7 MHz.

Table 34. LCD Data Requirements with 70 Hz Refresh, Internal LCD Clock, and ARM720T Bandwidth

PANEL RESOLUTION WITH DATA REQUIREMENT		Frame Buffer (KB)	ATTAINABLE LCD DATA RATE			BUS BANDWIDTH NEEDED BY LCD			AVERAGE BANDWIDTH NEEDED BY LCD			BANDWIDTH LEFT FOR OTHER OPERATIONS			EFFECTIVE CPU FREQUENCY		
						SDRAM	EXT SRAM	INT SRAM	SDRAM	EXT SRAM	INT SRAM	SDRAM	EXT SRAM	INT SRAM	SDRAM	EXT SRAM	INT SRAM
Resolution H x V	Bits/Pixel		MPixels /s	MWords /s	MBursts /s	%	%	%	%	%	%	%	%	%	MHz	MHz	MHz
XGA: 1024 x 768 Requires 60.5526 Mpixels/s	1	96.0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	2	192.0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	4	384.0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	8	768.0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	16	1536.0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SVGA: 800 x 600 Requires 36.96 Mpixels/s	1	58.59	50	1.56	0.20	8.98	11.72	x	6.64	8.66	x	93.36	91.34	x	38.9	39.8	x
	2	117.19	50	3.13	0.39	17.97	23.44	x	13.28	17.33	x	86.72	82.68	x	37.5	37.8	x
	4	234.38	50	6.25	0.78	35.94	46.88	x	26.57	34.65	x	73.44	65.35	x	34.3	33.3	x
	8	468.75	50	12.50	1.56	71.88	93.75	x	53.13	69.30	x	46.87	30.70	x	26.0	20.2	x
	16	937.50	50	25.0	3.13	143.75	187.50	x	x	x	x	x	x	x	x	x	x
VGA: 640 x 480 Requires 23.6544 Mpixels/s	1	37.50	25	0.78	0.10	4.49	5.86	x	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	2	75.0	25	1.56	0.20	8.98	11.72	x	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x
	4	150.0	25	3.13	0.39	17.97	23.44	x	17.0	22.18	x	83.0	77.82	x	36.6	36.6	x
	8	300.0	25	6.25	0.78	35.94	46.88	x	34.0	44.35	x	66.0	55.65	x	32.2	30.3	x
	16	600.0	25	12.50	1.56	71.88	93.75	x	68.01	88.7	x	31.99	11.30	x	19.9	8.9	x
HVGA: 640 x 240 Requires 11.8272 Mpixels/s	1	18.75	12.5	0.39	0.05	2.25	2.93	1.27	2.13	2.77	1.20	97.87	97.23	98.80	39.9	41.0	57.5
	2	37.50	12.5	0.78	0.10	4.49	5.86	x	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	4	75.0	12.5	1.56	0.20	8.98	11.72	x	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x
	8	150.0	12.5	3.13	0.39	17.97	23.44	x	17.0	22.18	x	83.0	77.82	x	36.6	36.6	x
	16	300.0	12.5	6.25	0.78	35.94	46.88	x	34.0	44.35	x	66.0	55.65	x	32.2	30.3	x
QVGA: 320 x 240 Requires 5.9136 Mpixels/s	1	9.38	5.55555	0.17	0.02	1.0	1.30	0.56	1.06	1.39	0.60	98.94	98.61	99.40	40.1	41.3	57.6
	2	18.75	5.55555	0.35	0.04	2.0	2.60	1.13	2.13	2.77	1.20	97.87	97.23	98.80	39.9	41.0	57.5
	4	37.50	5.55555	0.69	0.09	3.99	5.21	x	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	8	75.0	5.55555	1.39	0.17	7.99	10.42	x	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x
	16	150.0	5.55555	2.78	0.35	15.97	20.83	x	17.0	22.18	x	83.0	77.82	x	36.6	36.6	x
1/8 VGA: 320 x 120 Requires 2.9568 Mpixels/s	1	4.69	2.77777	0.09	0.01	0.50	0.65	0.28	0.53	0.69	0.30	99.47	99.31	99.70	40.2	41.4	57.6
	2	9.38	2.77777	0.17	0.02	1.0	1.30	0.56	1.06	1.39	0.60	98.94	98.61	99.40	40.1	41.3	57.6
	4	18.75	2.77777	0.35	0.04	2.0	2.60	1.13	2.13	2.77	1.20	97.87	97.23	98.80	39.9	41.0	57.5
	8	37.50	2.77777	0.69	0.09	3.99	5.21	x	4.25	5.54	x	95.75	94.46	x	39.4	40.4	x
	16	75.0	2.77777	1.39	0.17	7.99	10.42	x	8.50	11.09	x	91.50	88.91	x	38.5	39.2	x

**NOTES:**

- Internal SRAM: 32KB
- AHB Frequency: 50 MHz
- Burst size: 8 Words
- CLCD FIFO Fill Trigger → AHB Request: 1 Cycle
- AHB Request → Start AHB Access: 3 Cycles
- CLCD FIFO Data Load from AHB: 1 Cycle
- SDRAM burst: 23 Cycles (Controller input delay: 2 Cycles; Close old bank: 2 Cycles; Open new bank: 2 Cycles; CAS latency: 2 Cycles; Controller output delay: 2 Cycles)
- ARM SDRAM Controller is used
- Ext SRAM burst: 30 Cycles (Each word access: 3 Cycles; First word Overhead: 1 Cycle)
- ARM Static Memory Controller is used.
- Int SRAM burst: 13 Cycles
- CPU Speed 75 MHz
- Cache Hit/Miss Rate: 85%/15%
- ARM 720T Delay: 2 CPU Cycles
- AHB Wrapper Delay: 1 AHB Cycle
- Async Mode Delay: 2 1/2 CPU and 1/2 AHB Cycles
- All CPU accesses are cache line fills. (Burst size: 4; SDRAM burst: 14 Cycles; Ext. SRAM burst: 13 Cycles; Int. SRAM burst: 4 Cycles)
- MMU Hit Rate: 100.0%  
Effective CPU Frequency (MAX.): SDRAM: 40.3 MHz;  
External SRAM: 41.5 MHz; Internal SRAM: 57.7 MHz.

## CONCLUSION

LCD panels require an external controller to handle bias and clocking tasks, in addition to the constant stream of pixel data to be fed to the LCD. Instead of using a specific LCD driver IC to handle these tasks, the SHARP LH79520 System-On-Chip (ARM 722T core with a maximum CPU speed of 75 MHz and Bus speed of 50 MHz) has a built-in LCD controller to interface to most types of LCDs. This built in LCD controller offers a complete functionality — it can drive STN (single and dual scan), TFT and HR-TFT displays with sizes up to 800 × 600 (although limited by the memory bandwidth, the controller can drive even larger LCDs). This LCD controller can output data in widths from 1 bit to 24 bits, which corresponds to a color depth of 2, 4, 16, 256, 32,768 (5 bits per color in HR-TFT) and 262,144 (6 bits per color in TFT mode). This LCD controller can also work in palette mode (16-color or 256-color) and the internal palette table inside the SoC gives the ability to change the color by just changing the palette table.

When debugging, make sure the clock signal, the horizontal synchronization signals and the vertical synchronization signals are correct. Also make sure the LCD panel supply voltages are correct. Once these have been verified, then look to the configuration register values.

Frequently, the cause of 'no output on the LCD' lies with an incorrect sync signal polarity, or the wrong clock frequency being fed to the LCD. The front porch and back porch values are not that critical. Output should be visible on the LCD even though the back porch and front porch values aren't perfect.

Once all the signals have been straightened out, and the output on the LCD is acceptable, it is a valuable exercise to play around with the configuration register values in a developer's environment to find the best picture quality and position.

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**SHARP®****NORTH AMERICA**

SHARP Microelectronics of the Americas  
5700 NW Pacific Rim Blvd.  
Camas, WA 98607, U.S.A.  
Phone: (1) 360-834-2500  
Fax: (1) 360-834-8903  
www.sharpsma.com

**EUROPE**

SHARP Microelectronics Europe  
Division of Sharp Electronics (Europe) GmbH  
Sonninstrasse 3  
20097 Hamburg, Germany  
Phone: (49) 40-2376-2286  
Fax: (49) 40-2376-2232  
www.sharpsme.com

**JAPAN**

SHARP Corporation  
Electronic Components & Devices  
22-22 Nagaike-cho, Abeno-Ku  
Osaka 545-8522, Japan  
Phone: (81) 6-6621-1221  
Fax: (81) 6117-725300/6117-725301  
www.sharp-world.com

**TAIWAN**

SHARP Electronic Components  
(Taiwan) Corporation  
8F-A, No. 16, Sec. 4, Nanking E. Rd.  
Taipei, Taiwan, Republic of China  
Phone: (886) 2-2577-7341  
Fax: (886) 2-2577-7326/2-2577-7328

**SINGAPORE**

SHARP Electronics (Singapore) PTE., Ltd.  
438A, Alexandra Road, #05-01/02  
Alexandra Technopark,  
Singapore 119967  
Phone: (65) 271-3566  
Fax: (65) 271-3855

**KOREA**

SHARP Electronic Components  
(Korea) Corporation  
RM 501 Geosung B/D, 541  
Dohwa-dong, Mapo-ku  
Seoul 121-701, Korea  
Phone: (82) 2-711-5813 ~ 8  
Fax: (82) 2-711-5819

**CHINA**

SHARP Microelectronics of China  
(Shanghai) Co., Ltd.  
28 Xin Jin Qiao Road King Tower 16F  
Pudong Shanghai, 201206 P.R. China  
Phone: (86) 21-5854-7710/21-5834-6056  
Fax: (86) 21-5854-4340/21-5834-6057  
**Head Office:**  
No. 360, Bashen Road,  
Xin Development Bldg. 22  
Waigaoqiao Free Trade Zone Shanghai  
200131 P.R. China  
Email: smc@china.global.sharp.co.jp

**HONG KONG**

SHARP-ROXY (Hong Kong) Ltd.  
3rd Business Division,  
17/F, Admiralty Centre, Tower 1  
18 Harcourt Road, Hong Kong  
Phone: (852) 28229311  
Fax: (852) 28660779  
www.sharp.com.hk  
**Shenzhen Representative Office:**  
Room 13B1, Tower C,  
Electronics Science & Technology Building  
Shen Nan Zhong Road  
Shenzhen, P.R. China  
Phone: (86) 755-3273731  
Fax: (86) 755-3273735